Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

1-24. (*canceled*).

25. (*currently amended*) A circular buffer control circuit, comprising

a first number of circular buffer start registers;

a first number of circular buffer end registers, each associated with a different one of the circular buffer start registers; and

circular buffer control logic including

means for comparing a pointer to [[an]] a first address stored in a selected one of the circular buffer end registers, and

means for restoring to a register file [[the]] a second address stored in the one of the circular buffer start registers associated with the selected circular buffer end register, if the pointer matches the first address stored in the selected circular buffer end register.

26. (*currently amended*) A circular buffer control circuit, comprising

a first number of circular buffer start registers;

a first number of circular buffer end registers, each associated with a different one of the circular buffer start registers; and

control logic that compares a pointer to [[an]] a first address stored in a selected one of the circular buffer end registers and restores to a register file [[the]] a second

address stored in the one of the circular buffer start registers associated with the selected circular buffer end register, if the pointer matches the first address stored in the selected circular buffer end register.

27. (*currently amended*) A digital signal processor ~~capable of executing looping instruction commands~~, comprising:

a register set; and

means for executing a loop of instructions ~~command~~ a ~~fixed~~ specified number of times [[on]] determined by a loop count value ~~number stored in the register set~~, including

first means for executing a ~~current~~ first instruction specified by address bits stored in a first portion of a first register ~~within~~ of the register set,

second means for decrementing [[a]] the loop count value stored in a second register ~~within~~ of the register set, and

third means for executing ~~another portion of the current~~ a second instruction specified by address bits stored in a second portion of the first register and a third register ~~within~~ of the register set.

28. (*currently amended*) The digital signal processor of claim 27, further including means for exiting the loop of instructions ~~command~~ when the loop count value ~~reaches~~ equals zero.

29. (*currently amended*) A digital signal processor ~~capable of executing looping instruction commands~~, comprising:

a register set; and

control logic that executes a loop of instructions ~~command~~ a ~~fixed~~ specified number of times [[on]] determined by a loop count value ~~number stored in the register set~~, wherein the control logic

executes a ~~current~~ first instruction specified by address bits stored in a first portion of a first register ~~within~~ of the register set,

decrements [[a]] the loop count value stored in a second register ~~within~~ of the register set, and

executes ~~another portion of the current~~ a second instruction specified by address bits stored in a second portion of the first register and a third register ~~within~~ of the register set.

30. (*currently amended*) The digital signal processor of claim 29, wherein the control logic exits the loop of instructions ~~command~~ when the loop count value ~~reaches~~ equals zero.

31. (*new*) The circular buffer control circuit of claim 25, wherein the circular buffer control logic further includes

means for modifying the pointer by a stride value.

32. (*new*) The circular buffer control circuit of claim 31, wherein the stride value is programmable.

33. (*new*) The circular buffer control circuit of claim 26, wherein the control logic modifies the pointer by a stride value.

34. (*new*) The circular buffer control circuit of claim 33, wherein the stride value is programmable.